BS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,099	02/12/2002	Tod Paulus	SILA:097	7258

7590 12/01/2004

O'KEEFE, EGAN & PETERMAN, L.L.P.
Building C, Suite 200
1101 Captial of Texas Highway South
Austin, TX 78746

EXAMINER	
LEE, JOHN J	

ART UNIT	PAPER NUMBER
2684	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,099	PAULUS ET AL.	
	Examiner	Art Unit	
	JOHN J LEE	2684	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,14-16,30 and 31* is/are rejected.

7)☒ Claim(s) *6-13,17-29 and 32-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/2/02,9/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on 12/2/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the informal drawings are not of sufficient quality to permit examination. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 3-5, 14-16, 30, and 31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et al. (US Patent number 5,859,878) in view of Hessel et al. (US Patent number 6,389,078).

Regarding **claim 1,** Phillips discloses that a receiver digital circuitry (Fig. 1 and column 7, lines 27 – 67). Phillips teaches that digital down converter circuitry (210 in Fig. 3A) configured to mix a digital input signal provided by a receiver analog circuitry (104 in Fig. 1) with a digital intermediate frequency (IF) local oscillator signal to generate a digital down converted signal (Fig. 8A and column 25, lines 60 – column 26, lines 40, where teaches digital down converter generates pairs of in-phase and quadrature phase data that frequency (digital intermediate frequency) downconverted to baseband via a sinusoid generator, referred to as a numerically controlled oscillator, which generates both in-phase and quadrature phase local oscillator signals and I and Q digital mixers). Phillips teaches that digital filter circuitry (230 in Fig. 8A) configured to filter the digital down converted signal to generate a filtered digital signal (Fig. 3A, 8A, column 10, lines 33 – 48, and column 24, lines 34 – 61, where teaches if serial data output from digital down converter is to be input to a programmable digital filter unit (PDFU), the field programmable gate array may then reformat the data output to be

consistent with input requirements for the PDFU). Phillips teaches that the digital filter circuitry (230 in Fig. 8A) provides a notch at a frequency (Fig. 8A and column 24, lines 34 – column 26, lines 15).

Phillips does not specifically disclose the limitation "the digital filter circuitry provides a notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry". However, Hessel teaches the limitation "the digital filter circuitry provides a notch at a frequency that corresponds to a residual DC offset of the receiver analog circuitry" (Fig. 58, 60 and column 42, lines 60 – column 43, lines 61, where teaches high pass filters, which follows can filter the unwanted DC offset, processes the signals to remove any DC offset). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Phillips system as taught by Hessel. The motivation does so would be to improve the quality of output signal from receiver circuit in communication transceiver system.

Regarding **claims 3, 16 and 31,** Phillips discloses that the digital filter circuitry provides the notch a frequency of the intermediate frequency local oscillator signal (column 25, lines 47 – column 26, lines 40 and Fig. 6, 8, where teaches digital down converter circuitry performs downconverting and decimating (reducing (subtracting) the sample rate) from input sampling rate by cooperating filters and oscillator).

Regarding **claims 4 and 15,** Phillips discloses that the digital circuitry provides the notch by using a notch filter circuitry (Fig. 9, 10 and column 27, lines 11 – column 28, lines 27).

Regarding **claim 5,** Phillips does not specifically disclose the limitation "the notch filter circuitry has one or more poles the locations of which are adjustable over an adjustment cycle of the notch filter circuitry". However, Hessel teaches the limitation "the notch filter circuitry has one or more poles the locations of which are adjustable over an adjustment cycle of the notch filter circuitry" (column 26, lines 12 – column 27, lines 10 and Fig. 41, 42, 44, where teaches determining commutator position of the polyphase filter for adjustment of symbol timing decisions, and the adjustment are made after the computation of the next sample after master registers has been loaded (adjustment cycle)). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Phillips system as taught by Hessel, provide the motivation to enhance filter operation for qualify output signal in radio communication system.

Regarding **claim 14,** Phillips and Hessel disclose all the limitation, as discussed in claim 1. Furthermore, Phillips further discloses that receiver analog circuitry (104 in Fig. 1) included within a first integrated circuit (Fig. 4), the receiver analog circuitry configured to receive and process a radio frequency input signal to generate a processed radio frequency signal (column 17, lines 39 – column 18, lines 13 and Fig. 4, where teaches receiver analog circuitry having an integrated circuit that receives and processes radio input signals and then generates processed radio frequency signals), the receiver analog circuitry further configured to use an analog to digital converter circuitry (106 in Fig. 1) to convert the processed radio frequency signal into a digital output signal (column 14, lines 50 – column 15, lines 13 and Fig. 1, 4, where teaches the analog to

digital converter receives and converts the processed radio signals for inputting to digital receiver circuitry). Phillips teaches that receiver digital circuitry (106 in Fig. 1), included within a second integrated circuit (Fig. 8A) and coupled to the receiver analog circuitry (104 in Fig. 1) within the first integrated circuit (see signal lines 224, 226, 103b in Fig. 1), the receiver digital circuitry (106 in Fig. 1) configured to receive and process the digital output signal (from analog to digital converter to input digital receiver circuitry see Fig. 8A) to generate a processed digital signal (column 24, lines 34 – column 25, lines 46, where teaches receiver digital circuitry, which coupled to receiver analog circuitry, receives digital signal from analog to digital converter and processes to generate processed digital signal), the receiver digital circuitry (106 in Fig. 1) further configured to provide a notch in a frequency spectrum of the processed digital signal (8B and column 25, lines 47 – column 26, lines 67).

Regarding **claim 30,** Phillips and Hessel disclose all the limitation, as discussed in claims 1 and 14.

Allowable Subject Matter

5. Claims 6-13, 17-29, and 32-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose "receiver digital circuitry comprises the location of the one or more poles of the notch filter circuitry are adjusted in an initial part of the adjustment cycle of the notch filter circuitry so that the notch filter circuitry tends

to settle quickly" as specified in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kato (US Patent number 6,294,952) discloses Quadrature Demodulator Quadrature Demodulation Method and Recording Medium.

Luz et al. (US Patent number 6,321,073) discloses Radio Telephone Receiver and Method with Improved Dynamic Range and DC Offset Correction.

Huang (US Patent number 6,324,231) discloses DC Offset Cancellation Apparatus and Method for Digital Demodulation.

Information regarding...Patent Application Information Retrieval (PAIR) system... at 866-217-9197 (toll-free)."

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John J. Lee** whose telephone number is **(703) 306-5936**. He can normally be reached Monday-Thursday and alternate Fridays from 8:30am-5:00 pm. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, **Nay Aung Maung**, can be reached on **(703) 308-7745**. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-4700.

J.L
November 23, 2004

John J Lee

NAY MAUNG
SUPERVISORY PATENT EXAMINER